AMENDMENTS TO THE CLAIMS

1-17 (canceled)

18. (currently amended) A stacked microelectronic device, comprising:

a first substrate of silicon, said first substrate having a top surface;

a first plurality of interconnect structures formed on at least a portion of the first substrate;

a layer of nonconductive compliant material formed on at least a portion of the top surface of the first substrate of silicon, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures; and

a second substrate of silicon with a second plurality of interconnect structures formed thereon, said first and second substrates ~~interconnect structures~~ configured such that at least a portion of the interconnect structures of said first and second substrates respectively are in physical contact.

19. (currently amended) The ~~apparatus~~ device of claim 18, wherein the ~~apparatus~~ device comprises a stacked chipset.

20. (currently amended) The ~~apparatus~~ device of claim 18, wherein the first and second substrates comprise integrated circuits.

21. (currently amended) The ~~apparatus~~ device of claim 18, wherein at least a portion of the first plurality of interconnect structures or the second plurality of interconnect structures comprise copper vias.

22. (currently amended) The ~~apparatus~~ device of claim 18, wherein the ~~complaint~~ compliant material substantially comprises a soft polymer.

23. (currently amended) The ~~apparatus~~ device of claim 18, wherein the ~~complaint~~ compliant material substantially comprises one of ~~the~~ polyimide, polybenzoxazole, photodefinable siloxane, novolak, or a polynorborene buffer.

24. (currently amended) The ~~apparatus~~ device of claim 18, wherein the compliant material comprises photodefinable and non-photodefinable materials.

25. (new) A stacked wafer structure comprising:

a first wafer having a first interconnect structure formed thereon;

a second wafer having a second interconnect structure formed thereon, the second interconnect structure bonded to the first interconnect structure; and

a nonconductive compliant material disposed adjacent to the first interconnect structure and the second interconnect structure and between the first wafer and the second wafer, the nonconductive compliant material structurally supporting the first wafer during thinning of the first wafer.

26. (new) The structure of claim 25, wherein the nonconductive compliant material comprise a polymer material.

27. (new) The structure of claim 25, wherein the nonconductive compliant material comprise a photodefinable material.

28. (new) The structure of claim 27, wherein the photodefinable material comprises polyimide, polybenzoxazole, a photodefinable siloxane, novolak, or a polynorborene buffer.

29. (new) The structure of claim 25, wherein the nonconductive complaint material is compressed.

30. (new) The structure of claim 25, wherein the nonconductive compliant material includes an adhesion promoter applied to a surface of the material.

31. (new) The structure of claim 25, wherein the nonconductive compliant material includes a chemically etched surface.

32. (new) A stacked wafer structure comprising:

a first semiconductor wafer;

a first dielectric layer formed on the first semiconductor wafer;

a first conductive interconnect formed on the first semiconductor wafer, the first conductive interconnect raised with respect to a first surface of the first dielectric layer;

a first layer of nonconductive compliant material deposited on the first dielectric layer and first conductive interconnect, a portion of the first layer of nonconductive compliant material selectively removed to expose the first conductive interconnect;

a second semiconductor wafer;

a second dielectric layer formed on the second semiconductor wafer;

a second conductive interconnect formed on the second semiconductor wafer, the second conductive interconnect raised with respect to a second surface of the second dielectric layer;

a second layer of nonconductive compliant material deposited on the second dielectric layer and second conductive interconnect, a portion of the second layer of nonconductive compliant material selectively removed to expose the second conductive interconnect,

wherein the exposed second conductive interconnect is bonded to the exposed first conductive interconnect and the first layer of nonconductive compliant material physically contacts the second layer of nonconductive compliant material providing structural support to the stacked wafer structure.

33. (new) The structure of claim 32, wherein at least a portion of the nonconductive compliant material is deformed by creeping of conductive material of at least one of the first conductive interconnect or second conductive interconnect.

34. (new) The structure of claim 33, wherein the conductive material comprises copper.

35. (new) A stacked wafer structure comprising:

a first semiconductor wafer;

a first dielectric layer formed on the first semiconductor wafer;

a first conductive interconnect formed on the first semiconductor wafer, the first conductive interconnect raised with respect to a first surface of the first dielectric layer;

a nonconductive photodefinable compliant material deposited on the first dielectric layer and first conductive interconnect, a portion of the nonconductive photodefinable compliant material selectively removed exposing a top surface of the first conductive interconnect and creating a space around the first conductive interconnect;

a second semiconductor wafer;

a second dielectric layer formed on the second semiconductor wafer;

a second conductive interconnect formed on the second semiconductor wafer, the second conductive interconnect raised with respect to a second surface of the second dielectric layer,

wherein the second conductive interconnect is bonded to the exposed top surface of the first conductive interconnect and the nonconductive compliant material physically contacts the second dielectric layer providing structural support to the stacked wafer structure.

36. (new) The structure of claim 35, wherein the nonconductive compliant material is deformed into the space created around the first conductive interconnect when the second conductive interconnect is bonded to the exposed top surface of the first conductive interconnect.

37. (new) The structure of claim 35, wherein a surface of the nonconductive compliant material physically contacting the second dielectric layer is treated to improve adhesion properties of the compliant material.